CONTROL SYSTEMS AND METHODS

BACKGROUND OF THE INVENTION

The present invention relates generally to control systems for position sensing, and more specifically, to detecting faults in linear variable differential transformers and rotary variable differential transformers.

Position sensors are utilized in many different applications, including in gas turbine engines for aeronautical, marine, and industrial applications. Such engines often include, for example, rotary voltage differential transducers (RVDTs) and linear voltage differential transducers (LVDTs). The transducers are coupled to actuators, and provide a voltage signal proportional to a stroke position of the actuator.

To detect faults in RVDTs and LVDTs, a range test can be performed on the sum of secondary voltages from the transducers. A range test also can be performed on a sensed position to verify signal integrity. The range limits, however, must be set wide enough to account for all worse-case system variations. Otherwise, a properly operating transducer may be identified as having a fault. These wide range limits result, however, in detecting only extreme faults due to electrical open circuits or short circuits. Failures which cause only minor shifts in the sensed position value may not necessarily be detected, even though such failures can impact control system operation.

BRIEF SUMMARY OF THE INVENTION

Methods and systems for detecting faults in RVDTs and LVDTs are described. In an exemplary embodiment, a sum of secondary voltages V1 and V2 from a transducer is obtained by adding the secondary voltages together, i.e., V1 + V2. This sum of secondary voltages theoretically should be constant for all LVDT / RVDT positions, since the total length of the secondary transformer is constant. An electrical fault in the primary or secondary windings generates a corresponding change in the

sum of secondary voltages. By comparing this shifted value to a reference value which is representative of a no-fault condition, an error value is created which indicates the magnitude of the shift in the sum of the secondary values.

Depending upon the magnitude of the error value, certain actions are taken. For example, if the error value is above a first threshold, then the reference value representative of a no-fault condition is maintained constant. If the error value is above a second threshold, then a fault indication signal is generated. If the error value is between the first and second threshold values, then a confidence factor is generated which indicates the confidence level that a fault has occurred.

BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1 is a schematic illustration of a secondary winding of an LVDT and an RVDT;

Figure 2 is a schematic illustration of determining a value representative of whether a fault has occurred in an LVDT/RVDT; and

Figure 3 is a graph illustrating values of an exemplary confidence factor.

DETAILED DESCRIPTION OF THE INVENTION

Generally, as shown in Figure 1, an LVDT includes a secondary winding 10, and a movable core 12 within the LVDT that affects the output voltages V1 and V2. The sum of the voltages V1 and V2, however, remains constant provided there are no faults in windings 10. A secondary winding of an RVDT is configured identical to secondary winding 10 shown in Figure 1.

In accordance with one embodiment of the present invention, a sum of secondary voltages V1 and V2 is obtained by adding the secondary voltages together, i.e., V1 + V2. Again, this sum of secondary voltages theoretically should be constant for all LVDT / RVDT positions, since the total length of the secondary transformer is constant. An electrical fault in the primary or secondary windings will generate a

corresponding change in the sum of secondary voltages. By comparing this shifted value to a reference value which is representative of a no-fault condition, an error value is created which indicates the magnitude of the shift in the sum of the secondary values.

There are many possible logic circuits that could be used to determine whether the sum of secondary voltages indicates an error in the LVDT or RVDT. Figure 2 is a schematic illustration of one exemplary circuit 50 that can be used. The logic illustrated in Figure 2 can, for example, be implemented in an on-board interface board electrically connected between a transducer and a controller. Alternatively, the logic circuit could form part of an on-board controller.

More specifically, and referring to Figure 2, the secondary voltages from a transducer are denoted as V1 and V2. The summed value, V1 + V2, is fed to two separate simple one pole lag filters, i.e., a short term filter 52 and a long term filter 54. Short term filter 52, in an exemplary embodiment, has a time constant of 0.150 seconds. The output of short term filter 52 is summed signal V1 + V2 with high frequency noise removed and represents the current value of V1 + V2.

Short term filter 52 includes a multiplier 56 which multiplies the summed value by a short term weight factor 58. In an exemplary embodiment, the short term weight factor KST is 0.1. The weighted sum is then added at a summer 60 with a weighted value from a most previous sum. Specifically, the most previous short term sum value 62 is multiplied at a multiplier 64 by a weighting factor 66. In the exemplary embodiment, this weighting factor is 0.9. This weighted value is added at summer 60 with the current weighted value to provide a short term sum value. This current short term sum value is supplied to a summer 68. The current short term sum value also is stored in memory so that it can be used in determining the next current short term sum value.

Long term filter 54, in an exemplary embodiment, has a time constant of 30 seconds. The output of long term filter 54 represents the recent non-faulted

reference value of V1 + V2. In long term filter, switch S normally is in the position shown, i.e., position 0.

More specifically, long term filter 54 includes a multiplier 70 which multiplies the summed value by a long term weight factor 72. In an exemplary embodiment, the long term weight factor KLT is 0.0005. The weighted sum is then added at a summer 74 with a weighted value from a most previous sum. Specifically, the most previous long term sum value 76 is multiplied at a multiplier 78 by a weighting factor 80. In the exemplary embodiment, this weighting factor is 0.9995. This weighted value is added at summer 74 with the current weighted value to provide a long term sum value. This long-term sum value is supplied to summer 68. The current long term sum value also is stored in memory so that it can be used in determining the next current short term sum value.

Again, the output of short term filter 52 is continuously summed 68 with the output of long term filter 54. An absolute value 82 of this sum is obtained and is designated as DLTST (i.e., difference between long term and short term filters 52 and 54. Depending upon the value of DLTST, certain actions may be taken as described below.

Specifically, in an exemplary embodiment, if the absolute value of DLTST exceeds 0.05 Vrms, then the output of long term filter 54 should be frozen, i.e., a control signal 84 should transition switch S from position 0 to position 1. This results in freezing the value of long term filter and the reference value from long term filter 54 remains constant, i.e., value 76. This relationship is represented below.

If DLTST > LTfreezeThresh

Then LTfreeze = 1

Else LTfreeze = 0,

where, LTfreezeThresh = 0.05

If the absolute value of DLST exceeds 0.08 Vrms, then a fault indication VDTFLT should be set. This relationship is represented below.

If DLTST > V1 + V2FLTThresh,

Then VDTFLT = 1,

Else VDTFLT = 0,

where, V1 + V2FLTThresh = 0.08

If the absolute value of DLST is less than 0.08, the fault indication should not be set. As the absolute value of DLTST changes between 0.04 and 0.08, a confidence factor is generated which varies between 1.0 and 0.0, respectively. For absolute values of DLST less than 0.04 Vrms, the confidence factor should be 1.0, e.g., confident that no fault has occurred. For absolute values of DLTST values greater than 0.08 Vrms, the confidence factor should be 0.0, e.g., not confident that no fault has occurred. The confidence factor can be utilized in a control system to minimize the effect of an LVDT / RVDT failure.

An exemplary confidence factor is illustrated in a graph shown in Figure 3. As shown in Figure 3, when the Vrms value of the absolute value of DLTST is less than CFHiThresh, then a confidence value of 1 is assigned. When the Vrms value of the absolute value of DLTST is greater than CFLoThresh, then a confidence factor of 0 is assigned. For values between CFHiThresh and CFLoThresh, a linear relationship between the Vrms value and the confidence factor is provided. Exemplary values of CFHiThresh and CFLoThresh are set forth below.

CFHiThresh = 0.04

CFLoThresh = 0.08

While the invention has been described in terms of various specific embodiments, those skilled in the art will recognize that the invention can be practiced with modification within the spirit and scope of the claims.